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10EC63

Sixth Semester B.E. Degree Examination, June/July 2017
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer Three questions from Part A and Two from Part B.***

PART – A

1 a. Draw the i_D-V_{DS} characteristics of a enhancement MOSFET. Indicate the all regions of operation and explain it. **(07 Marks)**

b. For the circuit shown in Fig. Q1 (b), derive the expression of voltage gain, overall voltage gain, input impedance and output impedence. **(10 Marks)**

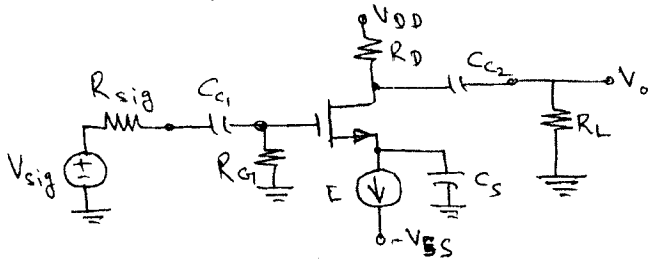

Fig. Q1 (b)

c. An nMOS transistor has $V_{to} = 0.8$ V, $2\phi_f = 0.7$V and $\gamma = 0.4\ V^{\frac{1}{2}}$. Find V_t when $V_{SB} = 3$ V **(03 Marks)**

2 a. The high frequency response an amplifier is characterized by the transfer function,

$$F_H(s) = \frac{1-\frac{s}{10^5}}{\left(1+\frac{s}{10^4}\right)\left(1+\frac{s}{4\times10^5}\right)}$$. Determine the 3-dB frequency. **(04 Marks)**

b. Explain the operation of a current mirror using MOSFET. **(08 Marks)**

c. Draw the circuit diagram to generate a number of constant currents of various magnitudes using BJT and explain it. **(08 Marks)**

3 a. Draw the circuit of a common gate amplifier with active load and explain it. **(07 Marks)**

b. What is cascade amplifier? Mention the advantages of it. **(04 Marks)**

c. Consider a common gate amplifier specified as follows : $\frac{W}{L} = \frac{7.2\,\mu m}{0.36\,\mu m}$,

$\mu_n C_{OX} = 387\ \mu A/V^2$, $\gamma_0 = 18\,K\Omega$, $I_D = 100\ \mu A$, $g_m = 1.25\,mA/V$, $\psi = 0.2$, $R_S = 10\,K\Omega$, $R_L = 100K\Omega$, Cgs = 20fF, Cgd = 5 fF and $C_L = 0$. Find A_{VO}, R_{in}, R_{out}, G_V, G_{IS} and G_I. **(09 Marks)**

4 a. Explain the operation of a MOS cascade amplifier. **(06 Marks)**

b. What is the need for transistor pairings? Draw all transistor pairings and mention advantages of each. **(08 Marks)**

c. Derive the expression of CMRR of a MOS differential amplifier for the two different cases. **(06 Marks)**

PART – B

5 a. Explain the operation of a active loaded MOS differential pair. **(08 Marks)**

b. Why differential amplifiers are well suited for IC fabrication? **(04 Marks)**

c. With neat circuit diagram, explain the operation of two-stage CMOS op-amp circuit. **(08 Marks)**

6 a. With a mathematical analysis, explain the effect of negative feedback on gain desensitivity and bandwidth extension. **(08 Marks)**

b. Draw the structure of a series-shunt feedback amplifier and derive the expression of input and output impedance with feedback. **(08 Marks)**

c. Draw the Root locus diagram for an amplifier with three poles and explain it. **(04 Marks)**

7 a. For the circuit shown in Fig. Q7 (a), determine the values of V_i, i_1, i_2, V_o and i_L. Also determine the voltage gain $\frac{V_0}{V_i}$, current gain $\frac{i_L}{i_i}$ and Power gain $\frac{P_0}{P_i}$. **(07 Marks)**

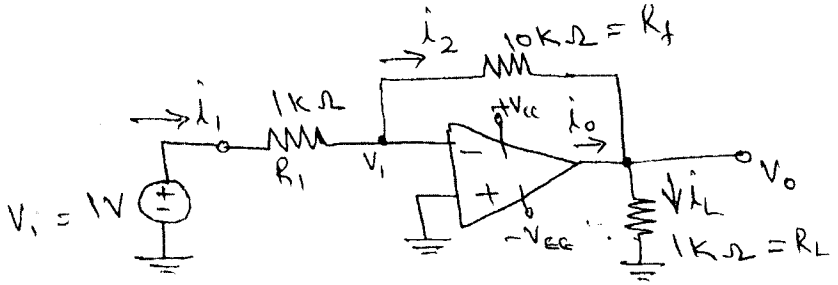

Fig. Q7 (a)

b. Derive the output voltage expression of a logarithmic amplifier with temperature compensation. **(09 Marks)**

c. With the help of waveform, explain the effect of slew rate limiting on output sinusoidal waveform. **(04 Marks)**

8 a. Define the following performance parameter of a logic circuit family and also draw the propagation delay and switching times waveform of the logic inverter.

(i) Noise margin

(ii) Propagation delay.

(iii) Robustness.

(iv) Delay-power product. **(10 Marks)**

b. Implement the following expressions using AOI gates and also write logic equivalent circuit

(i) $F = \overline{(A + B)(C + D)}$

(ii) $F = \overline{XY + \overline{Z}}$ **(10 Marks)**

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